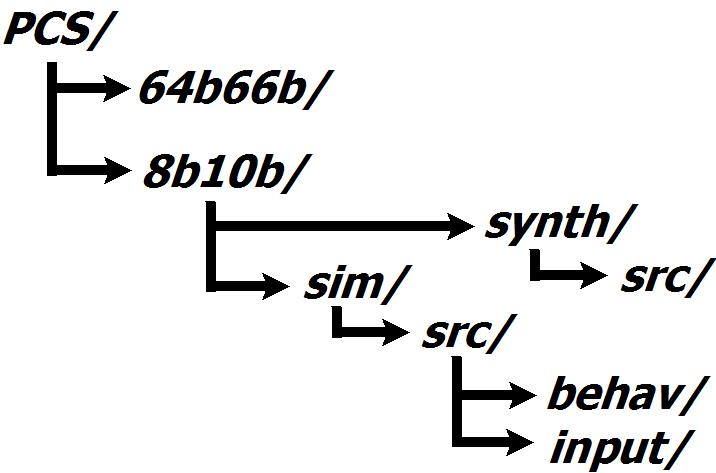
Code structure PCS/



Physical Coding Sublayer

Physical Coding Sublayer defines specifications for Physical Layer data encoding of a transmission system. 10Gbps transceiver implementation presented as a part of toolkit implementation uses two popular encoding schemes in its design: a DC-balanced 8b10b line code (1), and (2) a low-overhead scrambler-based 64b66b codec.

1. 8b10b

8b10b coder represents a class of parity-disparity DC-balanced codes that maps arriving 8-bit symbols into 10-bit code words using predefined code groups [1]. The code has a limited run length of identical symbols and guarantees the required transition density by means of extra redundancy bits. Sequence classification, disparity control and data encoding is performed at run time on the word-by-word basis.

The transmission part of 8b10b PCS is presented by the encoding block, which can be implemented either as an 8b10b unit operating at 1.25GHz clock frequency and 8-bit wide data interface, or as a dual 8b10b encoder (16b20b unit) operating at 625MHz and 16-bit wide interface. The implementation of the latter design defines a set of optional inputs, allowing the forced control of running disparity for two separately encoded data words. 8b10b coder structure is presented in Figure 1, marked as (b) sections.

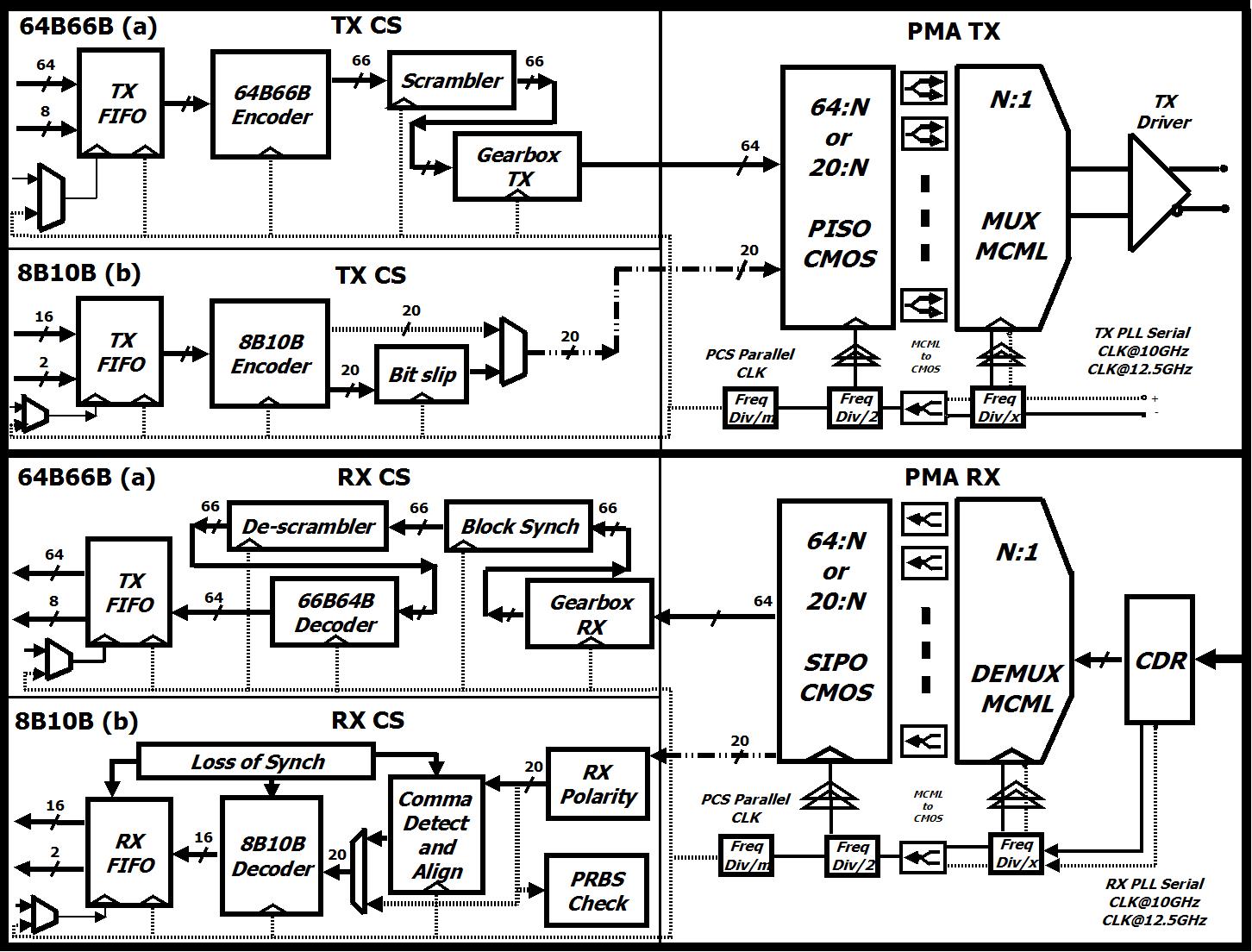


Figure 1. Top-level diagram of the transceiver design

The receiver of 16b20b design contains two identical decoders, a merge phase block, and a word alignment state machine that detects a certain number of input ordered sets arrived without errors. A set of asynchronous fifos is used to compensate the phase shift between the PCS module and the other external clock domains.

References:

[1] A. X. Widmer and P. A. Franaszek, “A DC-balanced, partitioned-block, 8B/10B transmission code,” IBM Journal of Research and Development, vol. 27, pp. 440–451, 1983.”

1. 64b66b

The reduction in baseband signalling rate of PHY is achieved in a hybrid-scrambled 64b66b encoding scheme. The encoding module performs a framing function by transforming the arriving combination of eight data octets, delimited by an 8-bit control word, into a 66-bit block of a certain structure specified in Figure 49-7 and Table 49-1 of IEEE std 802.3ae-2008 standard (Clause 49) [2]. 2-bit synchronization header is prepended to every encoded block on the basis of a block type being transmitted, and remains unscrambled throughout the transmission process. This property allows a simple frame detection/alignment process to be performed. A separate 64b66b scrambling block ensures statistical DC-balance of the encoded bit stream. The transition density of symbols is achieved via scrambling of frames' payload with a specific 58-th degree polynomial, which does not have any requirement for the initial seed value of the scrambler.

The top-level representation of 64b66b coding sublayer structure is shown in Figure 1, sections (a). The transmitter accepts an XGMII-formated 32-bit parallel word (followed by 4 control bits) at 312.5 MHz as an input and converts it into 66-bit words at 156.25MHz. As a rule, TX/RX datapaths have two internal parallel clock domain crossings between PCS and XGMII interfaces. All the phase differences that appear during the data transmission are compensated by asynchronous FIFO buffers, which have a built-it phase-alignment circuit.

64b66b PCS is presented by encoding/decoding module that performs 64-bit XGMII data mapping into 66-bit 10GBase-R representation (and vice versa) at 156.25MHz according to specifications of IEEE std 802.3ae-2008 standard [2]. Parallel scrambling unit stirs the payload within a clock cycle period to ensure sufficient transitions are provided for the clock recovery at the receiver side. Each 64-bit data word is scrambled with a 58th degree polynomial to ensure statistical DC-balance and transition density; 2-bit synchronization header is appended to allow frame detection and alignment to be performed. The transmission datapath widening is performed by a gearbox module, which handles 66-to-64 bits conversion between 156.25MHz and 161.13MHz clock domains. In addition to the datawidth conversion (161.13MHz 64bit words to 156.25MHz 66bit words) performed by the gearbox unit at the receiver side, the frame aligner synchronizes onto the 66-bit blocks by locking onto the position of the sync header.

References:

[2] IEEE 802.3ae. Part of IEEE Std 802.3-2008 (<http://www.ieee802.org/3/>).